Exercise 1

Suppose we have a computer that uses a memory address word size of 8 bits. This computer has a 16-byte cache with 4 bytes per block. The computer accesses a number of memory locations throughout the course of running a program.

Suppose this computer uses direct-mapped cache. The format of a memory address as seen by the cache is shown here:

Tag	Block	Word
4 bits	2 bits	2 bits

The system accesses memory addresses (in hex) in this exact order: 6E, B9, 17, E0, 4E, 4F, 50, 91, A8, A9, AB, AD, 93, and 94. The memory addresses of the first four accesses have been loaded into the cache blocks as shown below. (The contents of the tag are shown in binary and the cache "contents" are simply the address stored at that cache location.)

Block 0

Tag Contents	Cache Contents (represented by address)
1110	E0
	E1
	E2
	E3

Block 1

Tag Contents	Cache Contents (represented by address)
0001	14
	15
	16
	17

Block 2

Tag Contents	Cache Contents (represented by address)
1011	B8
	B9
	BA
	BB

Block 3

Tag Contents	Cache Contents (represented by address)
0110	6C
	6D
	6E
	6F

a) What is the hit ratio for the entire memory reference sequence given above?

b) What memory blocks will be in the cache after the last address has been accessed?

Exercise 2

A system implements a paged virtual address space for each process using a one level page table. The maximum size of virtual address space is 16MB. The page table for the running process includes the following valid entries (the → notation indicates that a virtual page maps to the given page frame, that is, it is located in that frame):

- Virtual page 2 → Page frame 4
- Virtual page 4 → Page frame 9
- Virtual page 1 → Page frame 2
- Virtual page 3 → Page frame 16
- Virtual page 0 → Page frame 1

The page size is 1024 bytes and the maximum physical memory size of the machine is 2MB.

a) How many bits are required for each virtual address?

b) How many bits are required for each physical address?

c) What is the maximum number of entries in a page table?

d) To which physical address will the virtual address 1524_{10} translate?

e) Which virtual address will translate to physical address 1024_{10}?

Exercise 3

Given a virtual memory system with a TLB, a cache, and a page table, assume the following:

- A TLB hit requires 5ns.
- A cache hit requires 12ns.
- A memory reference requires 25ns.
- A disk reference requires 200ms (this includes updating the page table, cache, and TLB).
- The TLB hit ratio is 90%.
- The cache hit rate is 98%.
- The page fault rate is .001%.

- On a TLB or cache miss, the time required for access includes a TLB and/or cache update, but the access is not restarted.
- On a page fault, the page is fetched from disk, all updates are performed, but the access is restarted.
- All references are sequential (no overlap, nothing done in parallel).

For each of the following, indicate whether or not it is possible. If it is possible, specify the time required for accessing the requested data.

a) TLB hit, cache hit

b) TLB miss, page table hit, cache hit

c) TLB miss, page table hit, cache miss

d) TLB miss, page table miss, cache hit

e) TLB miss, page table miss

Write down the equation to calculate the effective access time.